300-Watt, 100-kHz Converter Utilizes Economical Bipolar Planar Power Transistors

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APPLICATION NOTE

ABSTRACT

The continuous growth of SWITCHMODE™ Power Supplies (SMPS) worldwide makes this market one of the most important for manufacturers of power semiconductors. It is particularly important for manufacturers of devices in the 3 A to 10 A current range since most of these power supplies are designed to deliver power in the range of 50 to 1000 W. Although MOSFETs are often preferred for the new designs, ON Semiconductor has extended the capabilities of bipolar transistor products to meet the needs of the line operated SMPS with a series of economical bipolar transistors. This new series is in full production as the MJW180xx series which takes advantage of a planar process developed by ON Semiconductor.

This Application Note describes the design and performance a 300−W forward converter operating at 100 kHz utilizing the MJW18010 planar bipolar power transistor, and demonstrates the overall performance achievable with these new transistors.

LINE-OPERATED CONVERTERS

Voltage Requirements

The planar process is well established for small signal transistors; however, due to its limited breakdown voltage, it was not used to manufacture the high voltage devices needed to design line-operated SWITCHMODE Power Supplies.

For power supplies operating directly from the ac line, it can be seen from the standard equations of either the Flyback [1] or the Forward [2] converter topologies that high voltage devices are required. In single switch configurations, the BV_{ceo} of the transistor must be greater than 400 V, in conjunction with a minimum BV_{ces} of 800 V for circuits operating from a 220 V line. One can solve this problem by either using a collector-to-emitter clamp or using a dual switch design. The drawback will be higher cost and complexity of the total circuit; therefore, economical high voltage transistors are needed for single switch designs for these applications.

Flyback Converter: [1]

$$V_{CE(peak)} = \frac{N_p}{N_s}(V_{out} + V_f) + V_{spike}$$

Forward Converter: [2]

$$V_{CE(peak)} = V_{CC}\left(1 + \frac{V_{clamp}}{V_{CC}}\right)$$

where:

N_p = primary winding number of turns
N_s = secondary winding number of turns
V_{out} = output voltage
V_{CC} = DC supply for the converter, [$(\sqrt{2})(265)$ for a high 220 V line]
V_{spike} = uncontrolled voltage spike generated by the converter

Power supplies operating from a nominal line voltage of 220 V must be capable of operating from 265 V maximum, therefore, for the standard 5 V output, the $V_{CE(peak)}$ will be, in a first approximation, equal to 750 V, assuming that $N_p/N_s = V_p/V_s$ and $V_{clamp} = V_{CC}$.

PLANAR TRANSISTORS FOR LINE OPERATED CONVERTERS

In addition to high voltage capability, transistors for this application must have low conduction loss, fast speed and be economical. In the past, technologies such as triple diffusion and epitaxial collector with moats were used. These processes had sporadic yields and wide distributions of electrical characteristics. A planar process was developed in order to overcome these shortcomings.

Since the voltage capability of the planar process was a key issue, considerable design effort was focused on this parameter. The objective was to develop transistors capable of sustaining more than 1000 V in the BV_{ces} mode and yet maintain reasonable current gain and fast switching speeds.

A junction termination capable of sustaining over 1000 V was developed by putting a resistive field plate around the die. The cross section of a device utilizing this process is shown in Figure 1.

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High current gain, h_{FE}, lower $V_{CE(sat)}$ and tight switching time distributions are key characteristics for a transistor operating in a switching power supply and high carrier life time is needed to attain high h_{FE} and low $V_{CE(sat)}$. The inductive storage time of a transistor is a function of the carrier lifetime and the high lifetime process made this parameter worse. To overcome this drawback, a geometry with a high emitter perimeter/active area ratio was used to increase the speed of the transistors which enables fast−switching times. In addition, the masks of these new transistors are designed to optimize the base drive network, hence improving the dynamic performances.

The result of these development efforts is the MJE180xx and MJW180xx series of SWITCHMODE transistors.

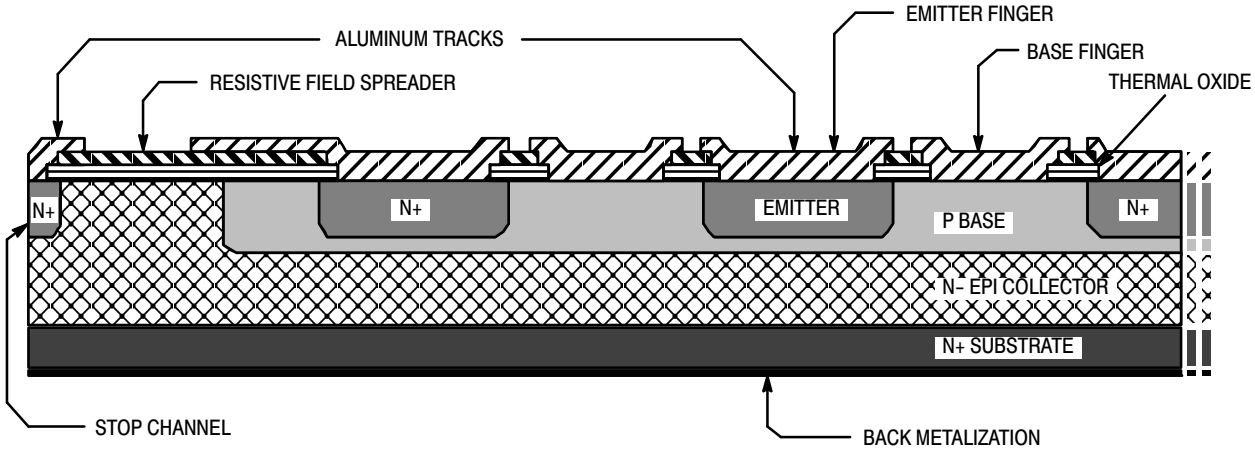


Figure 1. Cross Section of High−Voltage Planar Transistor

Current Gain Characteristics

To demonstrate the improvement in the gain characteristic of transistors fabricated with the planar technology, the electrical performance of similar transistors using a triple diffused process and epitaxial-collector diffusion were compared for electrical performance and parameter distributions.

The current gain of a power switch is a key characteristic. Both high gain and linearity are desirable characteristics of the planar transistor shown in Figure 2. The high h_{FE} at high collector current enables the transistors to be driven from standard integrated circuits even at high collector currents.

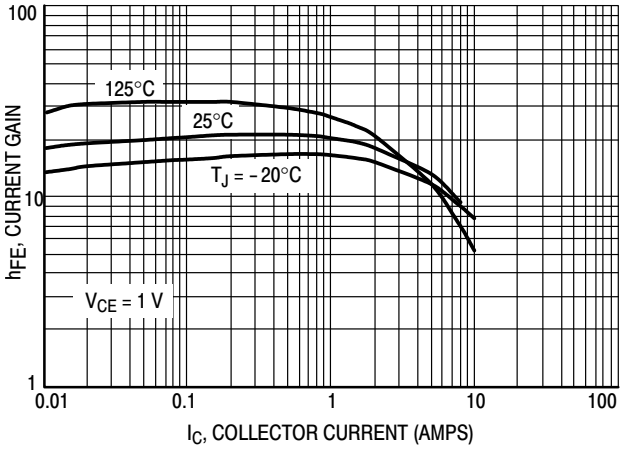


Figure 2. Typical Gain Curves for the Planar MJW18010

Tight distributions of h_{FE} allow designers of power supplies to design more efficient base−drive networks because it is no longer necessary for the base drive to handle wide distributions of current gain. Improvements of base−drive efficiencie,s by a factor of 3, can be achieved with these new planar transistors. Table 1 shows the statistical distributions of the current gain of transistors fabricated using three different processes. Note the tight distributions of the planar process.

Table 1.Statistical Distribution of Current Gain (h_{FE} @ I_C = 1 A, V_{CE} = 5 V)

Parameter	T_J = 25°C			T_J = 125°C		
	Triple Diff	Epi-coll	Planar	Triple Diff	Epi-coll	Planar
Mean	19.1	27.2	22.3	16.2	33.2	28.3
Std. Deviation	5.2	3.5	1.6	6.3	9	1.7
Minimum Value	12.1	17.2	20.0	18.1	25.8	25.4
Maximum Value	31.1	30.1	26.1	40.2	36.7	31.6

NOTE: Sample size: 50 parts

Turn−off Characteristics

The tight distribution of storage time distribution offers three main advantages.

1. Matching of the devices to build a quasi-resonant half−bridge converter is no longer required.
2. The dead time associated with the half− or full−bridge converter will be minimized, basically equal to the t_{si} range, yielding a much higher operating frequency than the one achievable with standard bipolar devices.
3. The performance of a given design is reproducible without tuning every circuit during the final check-out.

Based on the analysis performed on the turn−off parameters (Table 2), it's clear that the planar devices have a much lower spread than the other processes with a standard deviation approximately six times less than the triple diffused process.

Table 2.Statistical Distribution of Switching Time of High Voltage Transistors

Parameter	Storage Time t_{si} (μs)			Fall Time t_{fi} (ns)		
	Triple Diff	Epi-coll	Planar	Triple Diff	Epi-coll	Planar
Mean	1.68	1.19	1.27	57	71	39
Std. Deviation	0.29	0.05	0.05	10	8	3
Minimum Value	0.74	0.91	0.98	43	50	23
Maximum Value	2.19	1.29	1.33	86	90	44
Range	1.45	0.38	0.35	43	40	21

NOTE: Sample size: 50 parts

The switching performances are summarized by the curves given in Figures 3 and 4. It is worthwhile to note the high influence base drive conditions have on the switching speed for both storage and fall time. These figures indicate it is not good to drive the transistor into hard saturation because the switching times will significantly increase and the benefit of a low $V_{CE(sat)}$ will not compensate for the losses generated at turn-off. This is why it is necessary to use proportional base drive or a Baker clamp in power supplies which must operate from 10% to 100% of the rated output current.

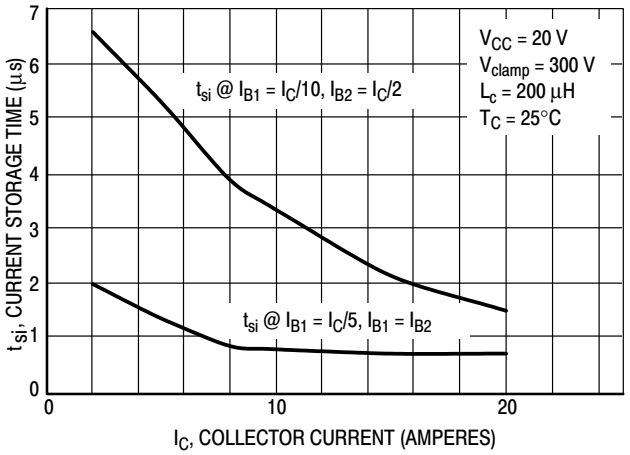


Figure 3. Collector Current Storage Time as a Function of I_C and Base Bias (MJW18010)

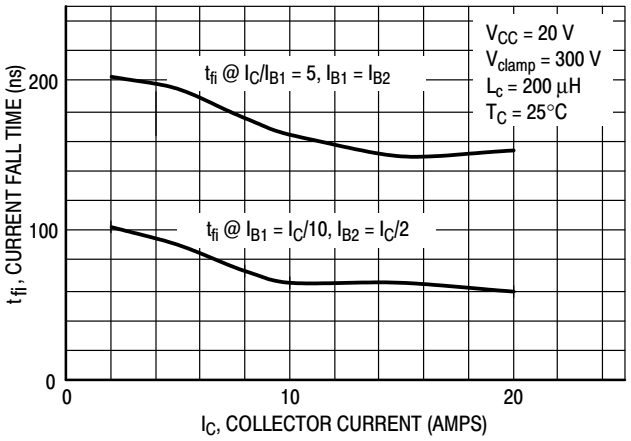


Figure 4. Collector Current Fall Time as a Function of I_C and Base Bias (MJW18010)

In this case, the collector current varies from less than 0.5 A up to 3.5 A. Without automatically limiting the base drive, the transistors would be driven into deep saturation with light loads and the switching times would be extremely slow.

The switching waveforms of the MJW18010 operating in a 300−W power supply are shown in Figures 5 and 6.

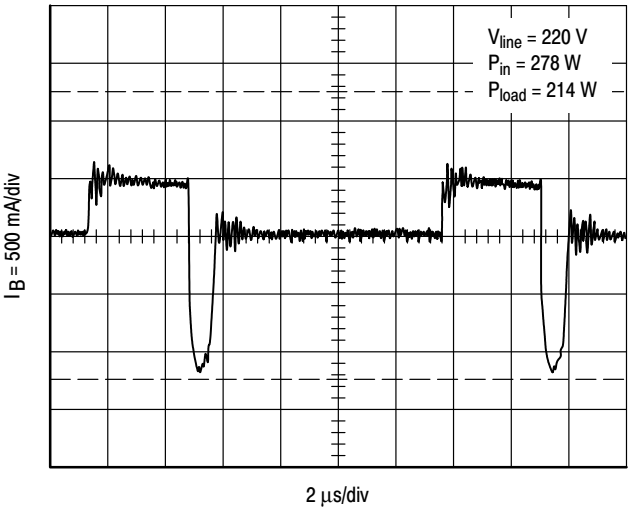


Figure 5. Base−Drive Waveforms of the MJW18010 in a 300−W Power Supply

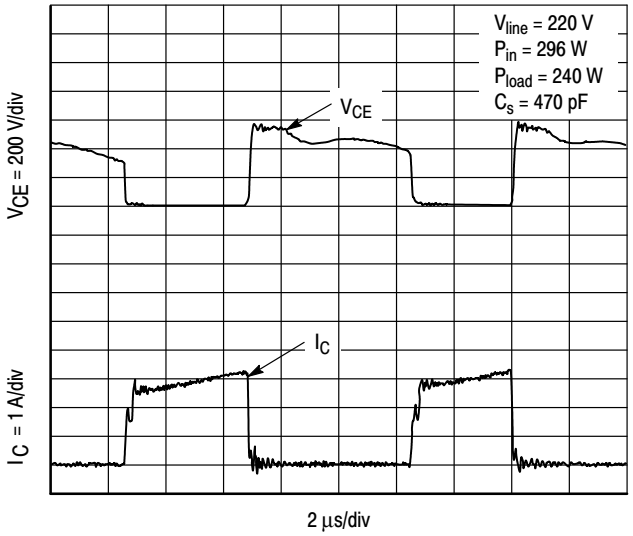


Figure 6. Collector Current and Collector−to−Emitter Voltage Waveforms of the MJW18010 in a 300−W Power Supply

APPLICATION OF THE PLANAR TRANSISTOR

Unlike the Flyback topology, the Forward converter (see Figure 7) transfers the energy from the primary to the load during the on time of transistor Q1. When Q1 is on, assuming the windings have the correct phase as indicated by the polarity dots, diode D1 is forward biased and the current can flow to the load thru inductor L_{out}. When the switch turns off, diode D1 is reverse biased, diode D2 turns on and yields the energy stored in the output inductance L_{out} to the load. D3, now forward biased, returns the magnetic energy (stored in the primary of transformer T1) back to the primary voltage source.

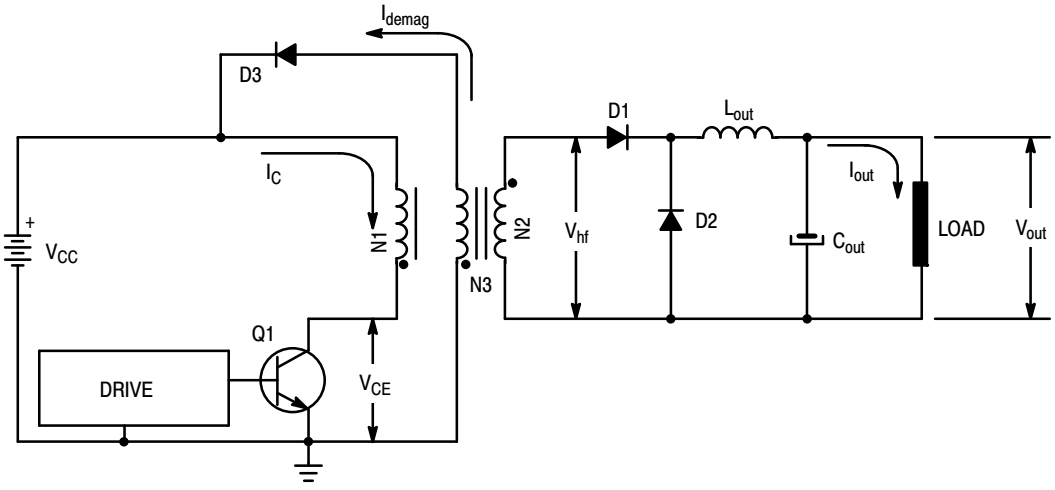


Figure 7. Basic Forward Converter Topology

The Forward topology is a little bit more complex than the Flyback circuit. An extra diode and a filter inductance in the output is required, in addition to a third winding and the associated diode to clamp the collector−to−emitter voltage. However, there is no need for a large gap in the core to store the energy prior to its transfer to the load. Therefore, the forward converter is well suited for low voltage, high current outputs. This configuration has four other major advantages which make it the right choice when the output power is above 200 W.

1. It behaves like a voltage source making the voltage regulation more simple, particularly when the load variation is large.
2. No load operation is possible at no extra cost.
3. The output transformer is smaller for the same output power than that of an equivalent Flyback inductor.
4. Output current ripple is much lower than the one of the Flyback, and the filtering of the output voltages is much easier.

The Forward topology was chosen for this application for these reasons.

DESIGN OF A 300−WATT OFF−LINE CONVERTER

The power supply was designed to meet the following specifications:

Input line voltage: 185 V min, 265 V max

Outputs: 5 V/30 A, minimum load = 3 A
100 V/1.5 A, minimum load = 0.15 A
Auxiliary: 15 V/0.3 A

Global efficiency ≥ 80%

Block Diagram

The block diagram of the converter is shown in Figure 8. The power supply was built using the MJW18010 for Q1 as the power switch, driven by the MC44602P2 current mode control IC. The output voltage was sourced from the rectifiers D8 and D9 associated with the passive components of the output network.

NOTE: All of the circuit description refers to the electrical schematic diagram of Figure 9.

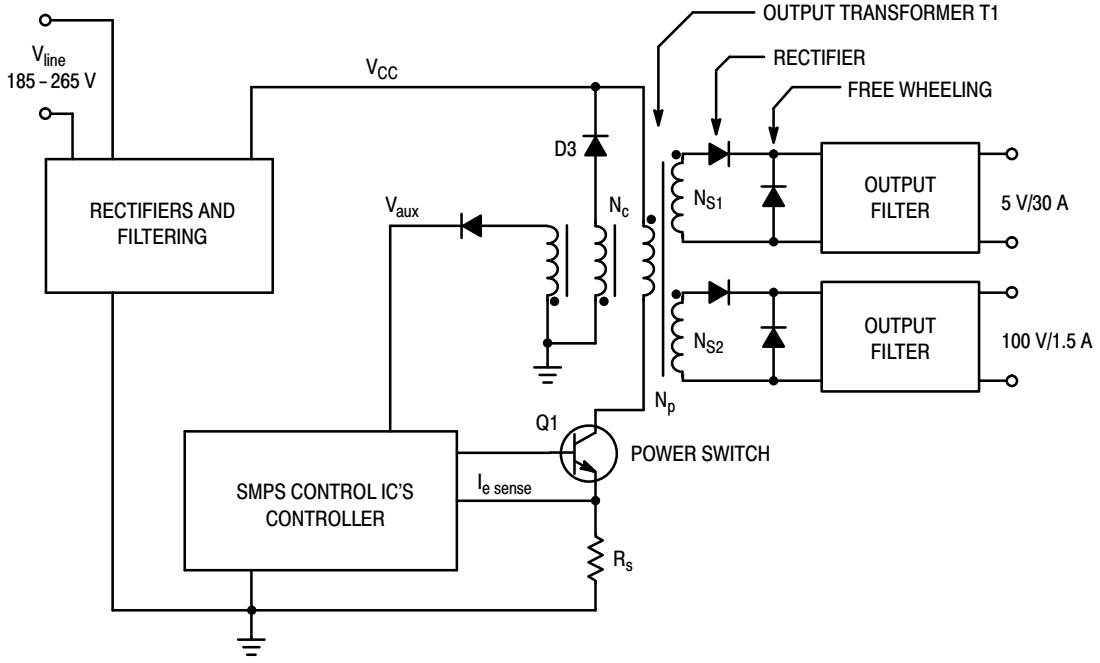


Figure 8. SWITCHMODE Power Supply Block Diagram

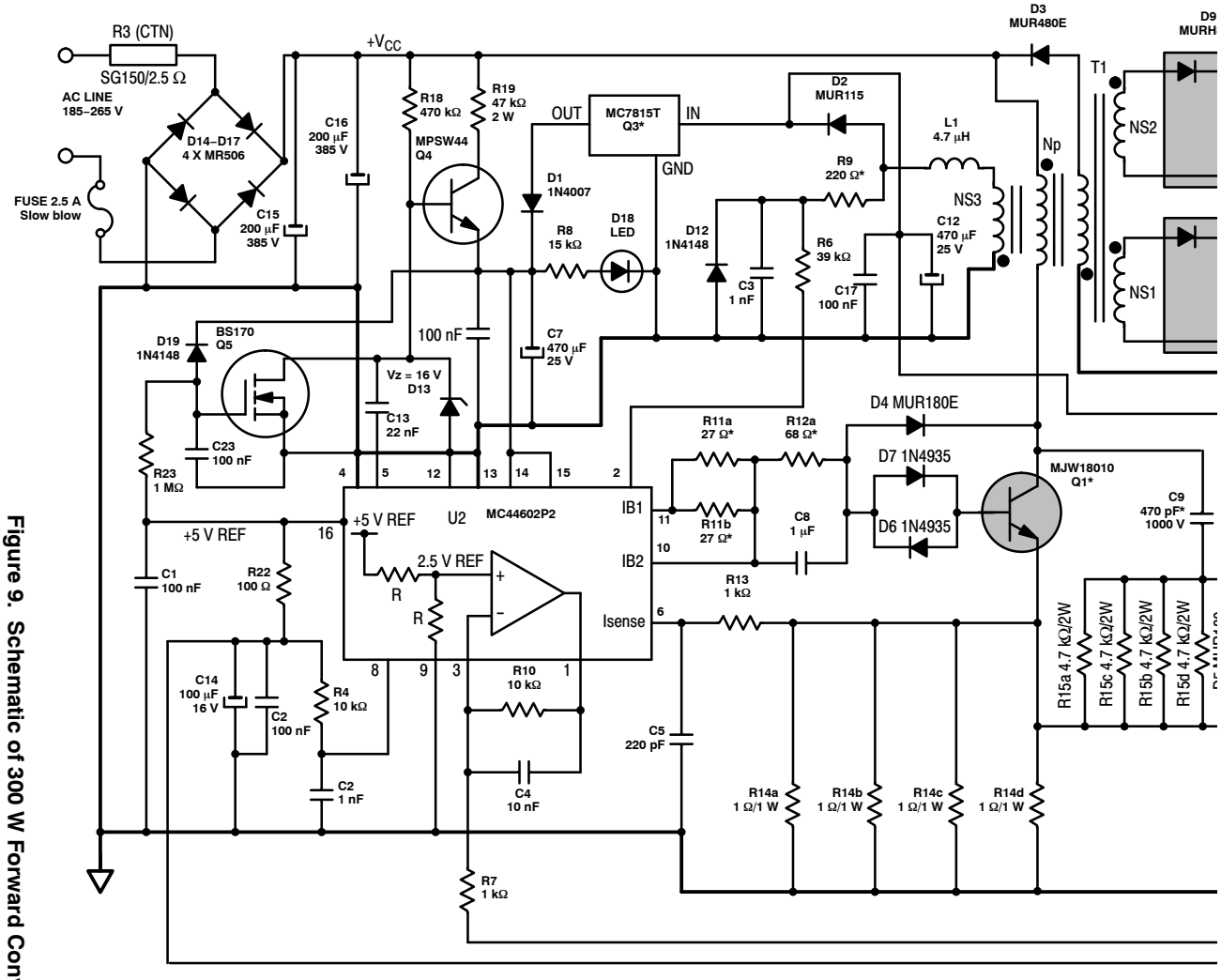


Figure 9. Schematic of 300 W Forward Converter

*Notes:

- all resistors are ±5%/0.25 W unless noted
- R11 & R12 (Base drive) are 0.5 W ± 5%
- R9 is 0.5 W ± 5%
- all capacitors are Polycarbonate, 63 V/±10% unless noted
- Q1 is mounted on a 5°C/W heatsink
- Q3 is mounted on a 20°C/W heatsink
- output diode D8 is mounted on a 3°C/W heatsink
- set jumper S1 to activate the Internal Voltage regulation
- set jumper S2 to activate the Opto-coupler Voltage regulation
- adjust V_{out} with P1 or P2 depending upon the Voltage regulation loop sele
- For lower current loads, D8 can be replaced by diodes in the TO-247 pack The MBR3045WT or MBR6045WT diodes are suggested replacements.
- C9 preferably polycarbonate
- RFI line filter not shown, but must be used on pc board.

Figure 9. Schematic of 300−W Forward Converter

Primary Side Operating Currents and Voltages Calculations

In order to simplify the manufacturing of the output transformer and to minimize the leakage inductance (which generates voltage spikes), the clamp winding N_c was made identical to the primary N_p. Therefore, the Collector−to−Emitter voltage, V_{CEpeak} voltage was twice the maximum V_{CC} value.

$$V_{CE(peak)} = 2\ V_{CC(max)} \qquad [3]$$

For a 220 V nominal line voltage, the maximum V_{CC} value is equal to 265 V, yielding a $V_{CE(peak)}$ of: $V_{CE(peak)} = 2\sqrt{2}(265) = 750$ V.

The collector current was directly dependent upon the output load. Under the worst case conditions, the $I_{C(peak)}$ is given by:

$$I_{C(peak)} = \frac{P_{out}}{\partial\ (V_{CC(min)})(DC_{max})} + I_{mag} \qquad [4]$$

with: P_{out} = maximum output power in Watts. ∂ = global efficiency in %.

$V_{CC(min)} = V_{CC}$ voltage under minimum V_{line}
DC_{max} = Maximum Duty Cycle
I_{mag} = Magnetizing current (I_{ripple})

The value of I_{mag} is specified by the designer; but as a general rule, I_{mag} is made equal to 10 to 20% of the output current (the I_{ripple} on the output) reflected back to the primary:

$$I_{mag} = I_{out}\ \frac{N_s}{N_p} \qquad [5]$$

In the case of multiple outputs, the higher output current value to compute I_{mag} is selected. The I_{ripple} is defined by the minimum load specified for that output.

Assuming an output current ripple of 20% of $I_{out(max)}$ and minimum voltage line of 185 V (as specified by the European normalization), then

$$I_{C(peak)} = \frac{300}{(080)(\sqrt{2})(185)(050)} + 057 = 340\ A$$

The primary current is sensed by R14 which is connected between the Emitter of Q1 and the ground line. Note that the current measured by this resistor is equal to I_e and must be sized accordingly. It is worthwhile to remember that for high current values, I_e cannot be assumed equal to I_c as shown by the following equation:

$$I_e = I_c + I_b \qquad [6]$$

The value of R14 is derived from the one volt internal current sense voltage reference of the MC44602P2. (See the MC44602P2 data sheet):

$$R14 = \frac{V_{ref}}{I_e} \qquad [7]$$

This resistor must be able to handle the power dissipated during the normal operation:

$$P_{R14} = (V_{sense})(I_e)(DC_{max}) \qquad [8]$$

It was necessary to use a low−pass filter connected between R12 and the current limit input of the driver (pin 6) since the practical current waveform was far from the ideal one as depicted by the oscillograms given in the measurement paragraph. The cutoff frequency must be well above the nominal chopper frequency of the converter; otherwise, the circuit will not work properly during the transient and overload conditions. Such a filter was designed with the R13/C5 network that will damp the spikes and avoid false triggering of current limit circuit.

From the above equations, and assuming a forced gain (β_f) of 10, then:

$$R14 = \frac{1}{34 + 034} = 026\ \Omega$$

and:

$P_{R14} = (3.40 + 0.34)\ 0.5 = 1.87$ W

Four 1 Ω/0.5 W resistors in parallel were used because it was a more economical than a single 0.25 Ω/2 W resistor.

The low pass filter was built with R13 = 1 kΩ and C5 = 220 pF, giving a time constant of 220 ns, well within one period of the converter, even at light load operation. However, since the spikes generated in the circuit are dependent upon the assembly and wiring techniques used to manufacture transformer T1, it may be necessary to tune this circuit during the final check of the power supply.

The Control Circuit

In conjunction with the development of the planar transistors, ON Semiconductor has designed the MC44602P2, an integrated circuit dedicated for SMPS. This IC is housed in a standard 16−pin dual in−line plastic package and can source up to 0.5 Ampere of current to the base of a bipolar transistor. The circuit can also be used to drive a MOSFET device.

The MC44602P2 includes the following features (please refer to the data sheet for a detailed analysis of the IC): current mode operation, built-in short-circuit detection with soft start and foldback characteristic, separated source/sink output pins to drive the bipolar transistors, duty cycle internally limited to 50%, internal oscillator up to 1 MHz and an extra pin to synchronize the oscillator on an external reference.

The driver operates as a constant frequency, pulse width modulation, current mode converter.

One advantage of the new ON Semiconductor power transistors is the elimination of an external negative supply to reverse bias the Base/Emitter junction at turn off. Since all of the diffusion parameters are under control (particularly the h_{FE}), there is no need to overdrive the transistor; therefore, the excess charges stored are minimum. The drive of the MJW180xx transistors is very simple; only a single low cost polycarbonate capacitor (C9) was needed to generate the negative voltage across the Base/Emitter junction. Due to the MC44602P2 sink capability of 2 A peak, the I_{B2} current can be optimized to achieve very fast switching times and keep the turn-off losses at a minimum.

A good compromise is to make $I_{B2} = I_{Cpeak}/2$. This will yield a very fast collector current fall time (t_{fi}) and short storage time (t_{si}). The dynamic performances can be improved by using a negative bias equal to the I_{Cpeak} value.

The voltage across C8, which is the V_{BEoff}, is derived from the value of the switching frequency, the V_{BB} voltage sourced from the driver and resistor R11. By using equation [12], one can determine the value of capacitor C8 used to reverse bias Q1:

$$V_{BEoff} = V_{BB}\,(1\text{-}e^{-t/T}) \qquad [9]$$

The time, t, is the minimum I_{B1} pulse width while T is the time constant R12/C8. Let $x = V_{BEoff}/V_{BB}$, then

$$x = 1\text{-}e^{-t/T} \qquad [10]$$

and:

$$e^{-t/T} = 1\text{-}x$$

The value of T is then given by equation [11]:

$$T = -\frac{t}{\ln(1 - x)} \qquad [11]$$

and C8 is derived from [12]:

$$C8 = \frac{T}{R12} \qquad [12]$$

The divider built with R11/R12 should not degrade the V_{BEoff} defined by the designer. Therefore:

$$\frac{R12}{R11 + R12} > \frac{V_{BEoff}}{V_{BB}}$$

The value of R12 can be approximated by equation [13] and refined during the final check of the prototype:

$$R12 = \frac{V_{BB}R11}{V_{BEoff}} \qquad [13]$$

It is possible to replace R12 with a zener diode; however, since the I_{B1} and I_{B2} currents might be quite large, this solution may not be economical for high power converters.

The forward bias of Q1 must force the operating point into the saturation region at maximum Icpeak current. Therefore:

$$\beta_f \leq h_{FEmin} \qquad [14]$$

with:

h_{FEmin} = minimum DC current gain at $I_C = I_{Cpeak}$
β_f = forced DC current gain selected by the designer

The value of I_{B1}, the forward base bias of Q1, is derived from the standard DC current gain equation:

$$I_{B1} = \frac{I_{C(peak)}}{\beta_f} \qquad [15]$$

NOTE: There is no major benefit to overdrive the transistor by selecting a forced gain well below the minimum h_{FE} for the transistor. As a rule of thumb, a β_f equal to 80% of the minimum h_{FE} specified for the MJW180xx products is suggested.

Computing R11 is straightforward with equation [16]:

$$R11 = \frac{V_{CC} - V_{sat_d} - V_{beQ1} - V_{f_{D7}} - V_s}{I_{B1}} \qquad [16]$$

Since the converter must operate at 10% of the maximum load, the collector current span will be very high and the transistor will either be overdriven under light load, or may operate in the quasi−saturation region under a full load condition. Compromises can be made with the β_f, but the performance of the transistor will be severely degraded under worst case conditions. The Baker clamp configuration consisting of D4, D6, and D7 was chosen. It is simple to implement, needs no adjustment and it is a low cost alternative. Diode D4 must be an ultra fast, high voltage type (because it must sustain the V_{CB} voltage), but D6 and D7 can be low voltage, fast rectifiers. All of these diodes are rated at forward current of 1 Ampere. Another option is to use a proportional drive by means of an extra transformer in the Emitter−to−Base network.

At start up, the V_{CC} supply is derived from the rectified line voltage and stabilized to 15 V by Q4 and the associated components. When the MC44602P2 becomes active, the 5 V reference is used to drive a small signal MOSFET (Q5) which, in turn, pulls the Base of Q4 to ground. This network is more complex than using a single high power resistor, but by disconnecting the line supply when the circuit is running, a few watts are saved, increasing the overall efficiency.

When the power supply operates in steady-state, V_{CC} is generated by the extra winding Nvaux, connected in Flyback, of the output transformer T1. This voltage is rectified by diode D2 and stabilized to 15 V by the linear post regulator Q3. Such a circuit is mandatory because the output voltages are all derived from a Forward topology. There is no way to achieve cross regulation between the main loop (built around the 5 V output) and the V_{CC}. Moreover, since the I_{B1} current is sourced from the V_{CC}, any variation of this voltage will influence the drive of Q1 and, hence, the global efficiency by the losses generated into the power transistor and the power loss in resistor R11. The V_{aux} winding is also used to sense a short−circuit condition, the AC voltage being applied to pin 2 by R6 and clamped to one V_f drop with diode D2. This voltage must be referenced from a flyback winding (see the MC44602P2 data sheet).

In order to take the full advantage of the modern standard ferrites without the limitation at high frequency of the passive components, the chopper frequency is set to 100 kHz with R4/C3. This operating frequency will minimize the size of the filter without the price of special parts to build the output transformer keeping the eddy current losses at a reasonable level.

The Output Transformer

As previously mentioned, the same number of turns for the primary and the clamp windings were used, the main advantages being a V_{CE} voltage limited to twice the maximum rectified line voltage, good magnetic coupling and duty cycle up to 50%. Since the converter was designed

to operate at 100 kHz, a ferrite material with minimum eddy losses under such frequency was selected. From the Thomson LCC data book, the B52 with a maximum operating frequency of 200 kHz material fits our application. Computing the minimum winding area needed to build the transformer allowed us to select the core shape from the standard "off the shelf" parts.

The turns ratio between the primary N_p and each secondary winding is calculated using equation [17]:

$$x_i = \frac{2V_{out}}{E_{min}} \quad [17]$$

Because of the 50% maximum duty cycle, twice the output voltage was used. Since the converter must supply the output voltage even under the minimum input line voltage, the Emin value was used to compute the N_p/N_s ratio.

Then:

$$x_1 = \frac{2(5)}{(\sqrt{2})(185)} = 0.038 \text{ for the 5 V output}$$

$$x_2 = \frac{(2)(100)}{(\sqrt{2})(185)} = 0.763 \text{ for the 100 V output}$$

$$x_3 = \frac{(2)(15)}{(\sqrt{2})(185)} = 0.114 \text{ for the } V_{aux} \text{ output}$$

For a Forward converter, the A_eA_w is given by equation [18]:

$$A_wA_e = [\frac{(k)(DC)(E_{max})}{(B_{max})(J_a)(F)}] \Sigma \quad [18]$$

Where:

$$\Sigma = 3\ [\sqrt{DC}\ \Sigma(x_i)(I_{oi}) + \sqrt{1 - DC}\ \Sigma(x_j)(I_{oj})]$$

k = winding factor, equal to 2

DC = maximum Duty Cycle in %
E_{max} = maximum rectified line voltage
B_{max} = maximum allowable flux in Tesla
J_a = current density in the windings
F = chopper frequency in Hertz
x_i = primary to secondary turn ratio for the Forward windings
I_{oi} = output current for the Forward windings
x_j = primary to secondary turn ratio for the Flyback winding (clamp winding is not included)
I_{oj} = output current for the Flyback windings.

Then:

$$\Sigma = 3\ [(\sqrt{0.5})\ [(0.763)(1.5) + (0.038)(30)] + \sqrt{0.5})(0.114)(0.3)] = 4.92$$

$$A_wA_e = [\frac{(2)(0.50)(265)(\sqrt{2})}{(0.20)(5)(10^5)}] \Sigma = 1.456 \text{ cm}^4$$

From the Thomson-LCC data book, the ETD49 core, with an AwAe factor of 5.7 cm^4, fits the application and provides a lot of room to perform some experiments during the final check and characterization of the SMPS and the associated components. The final circuit may be built with a much smaller core like the ETD39 from the same supplier.

The number of turns for the primary winding is given by equation [19]:

$$N_p = \frac{(E_{max})(DC_{max})}{(A_e)(B_{max})(F)} \quad [19]$$

then:

$$N_p = \frac{(265)(\sqrt{2})(0.50)}{(211E^{-6})\ (0.20)10^5} = 44 \text{ turns}$$

Assuming a current density of 5 A/mm^2, the wire diameter for N_p was 0.8 mm. Based on this value and the ratios calculated above, the number of turns for each secondary was calculated:

$N_{s1} = N_px_1 = (44)(0.038) = 1.67$
Wire diameter: use flat copper ribbon 1 mm x 1 cm

$N_{s2} = N_px_2 = (44)(0.763) = 34$ turns
Wire diameter = 1 mm

$N_{s3} = N_px_3 = (44)(0.114) = 5$ turns
Wire diameter = 0.2 mm

Since the current required is very high for the 5 V output, we'll use two turns for the N_{s1} secondary to take into account the IR loss in the winding. This increased the reverse voltage applied to the rectifiers associated to that output, but the ON Semiconductor portfolio of Schottky rectifiers offers a number of devices to fit the application.

The magnetizing current in the transformer was adjusted by setting the air gap in the center leg of the core. As discussed previously, Imag = 0.57 A.

The primary inductance is then given by equation [20]:

$$L_p = \frac{(E_{min})(DC_{max})}{(I_{mag})(F)} \quad [20]$$

Where:

L_p = primary inductance in Henries
E_{min} = minimum rectified input line voltage

$$L_p = \frac{(185)(\sqrt{2})(0.50)}{(0.57)(10^4)} = 230 \text{ mH}$$

Based on the data sheet published by the manufacturer of the ETD49 core, an air gap of 0.1 mm was used to get the required inductance.

Power Switch Selection

It is already stated that, at turn-off, the power transistor will be biased with a Collector−to−Emitter voltage of 750 V with a low Base/Emitter impedance. The transistor will switch from the off state to saturation from a V_{CC} voltage equal to 375 V. Based on these needs, and taking into account the uncontrolled voltage spikes (particularly those generated by the leakage inductance of the output transformer), the transistor must block 450 V in BV_{ceo} mode and 1000 V in BV_{ces} to be within the recommended 80% range of the maximum ratings for power transistors.

For the $I_{C(peak)}$ and the required current gain, we must select a device with an h_{FEmin} of 10 at I_C = 3.5 A, V_{CE} = 1 V, together with a nominal collector current capability of at least equal to I_{Cpeak}. The transistor must have FBSOA and RBSOA capabilities to handle the worst case conditions that may occur.

The MJW18010 with the following primary characteristic was selected:

BV_{ceo}: 450 V I_C max: 8 A
BV_{ces}: 1000 V I_C nom: 4 A
h_{FE} @ I_C = 4 A, V_{CE} = 1 V, T_J = 25°C 10 min

Since the transistor operates under an inductive load, it was necessary to use a snubber network to improve the global efficiency and to assure that, regardless of the transient condition, the operating point will never exceed the RBSOA limit of the MJW18010. The basic idea was to reduce the dv/dt at turn-off, which is reapplied across the Collector−to−Emitter of the transistor. This was easily achieved by means of a capacitor (C5) which is charged through D5 when the voltage rises, limiting the slope, and discharged with R15 when Q1 is turned on at the next cycle. To compute the value of capacitor C9, the designer must consider the turn-off time (t_{fi}) of Q1 and the peak voltage across the transistor as shown by equation [21]:

$$C_s = \frac{(I_{C(peak)})(t_{fi})}{V_{CE(peak)}} \quad [21]$$

$$C9 = \frac{(34)(100)(10^{-9})}{750} = 453 \text{ pF}$$

A standard 470 pF/1000 V polycarbonate type was selected to minimize the losses generated by the high frequency into the capacitor.

The capacitor must be fully discharged during the minimum on-time of Q1 with the discharge current by R15 to avoid any overload of the power switch.

Therefore, the value of R15 is given by:

$$R15 \leq \frac{DC_{min}}{4C_sF} \quad [22]$$

$$DC_{min} = DC_{max}\frac{E_{min}}{E_{max}}$$

then:

$$DC_{min} = 0.50\,\frac{185}{265} = 0.35$$

and

$$R15 \leq \frac{0.35}{(4)(470)(10^{-12})(10^4)} \leq 1860\ \Omega$$

The power dissipated by R15 is equal to the energy stored into C9 times the chopper frequency:

$$E_j = \frac{1}{2}C_s(V_{CE(peak)}^2) \quad [23]$$

$$P = E_jF \quad [24]$$

With the above snubber, the losses will be:

$$E_j = \frac{1}{2}(470)(10^{-12})(750^2) = 132\ \mu J$$

and:
$P_{off} = (132)(10^{-6})(10^4) = 13.2$ W

R15 consists of four 4.7 kΩ/4 W resistors in parallel as shown in the schematic diagram in Figure 9.

Diode Selections

Selecting the Baker Clamp diodes is straightforward and needs no detailed comments. The diode connected between Base/Collector must sustain the full V_{CEpeak}, the forward current being limited to I_{B1}. D4 is an Ultra−Fast, MUR180E. Diodes D6 and D7 are not as critical as D4; therefore, low cost medium V_{rm}, 1 A fast diodes like the 1N4935 were selected here. The selection of D3, MUR480E, located in the clamp network, is done by simply taking care of the 800 V V_{rm} capability together with a very fast t_{rr} (reverse recovery time) and t_{fr} (forward turn on time), the forward current being limited to the Imag as discussed in the previous paragraphs.

The Output Network

Prior to computing the value of the inductances needed in the output filters, one should set the output ripple current accordingly to the minimum load for each outputs. This ripple is derived from the minimum current needed to keep the operating point in the continuous mode. Based on the general specifications of the power supply, the 5 V output current was 3 A minimum and 0.15 A for the 100 V output.

The values of the inductors are derived from Lenz's law:

$$V = L\frac{di}{dt} \quad [25]$$

then:

$$L_{out} = \frac{(1 - DC_{max})V_{out}}{(F)(\Delta IL_{out})} \quad [26]$$

hence:

$$L_{o1} = \frac{(1 - 0.5)(100)}{(10^4)(0.15)} = 333 \text{ mH for the 100 V output}$$

$$L_{o2} = \frac{(1 - 0.5)(5)}{(10^4)(3)} = 83\ \mu H \text{ for the 5 V output}$$

The output capacitor values, computed with equation [27] to cope with the ripple voltage, ΔV_{out} is selected by the designer under the full load operation. Ripple voltages of 1% for the 5 V and 2% for the 100 V outputs were chosen.

$$C_{out} = \frac{\Delta I_L}{(\Delta V_{out})(8)(F)} \quad [27]$$

The equation doesn't take into account the capacitor equivalent series resistance (ESR) and, for high current

outputs, this resistance cannot be neglected. One should consider the dynamic operation of the circuit by determining the capacitors values from the damping factor of the output filters.

The damping factor [k] is given by equation [28]:

$$k = \frac{\sqrt{L_{out}}}{2(R_{out})(\sqrt{C_{out}})} \quad [28]$$

with:
R_{out}: output equivalent resistance = V_{out}/I_{out}

On the other hand, we can state that:

$$V_{out} = \frac{\Delta I_L \sqrt{L_{out}}}{\sqrt{C_{out}}} \quad [29]$$

This solution implies that a low L/C ratio to get a negligible ripple voltage results in a poor damping of the global system. One must make a compromise and it has been demonstrated that a damping factor k between 0.1 to 0.2 yields good results for large variations of the loads.

Taking k = 0.1 and $C = L_{out}/4(R_{out}^2)(z^2)$ then:

$R_{out} = 5/30 = 0.166\ \Omega$

$C_{o1} = (8.30)(10^{-6})/(4)(0.166^2)(0.1^2) = 7500\ \mu F$

$R_{out2} = 100/1.5 = 66.66\ \Omega$

$C_{o2} = (3.33)(10^{-3})/4(66.66^2)(0.1^2) = 18.7\ \mu F$

Two 4700 µF/16 V capacitors were used for the 5 V output and one 100 µF/200 V for the 100 V output.

Opto Loop Control

In order to provide full galvanic isolation from primary to secondary, the voltage regulation loop was made through an Optocoupler connected on the 5 V output. The output voltage, sensed by the resistive divider consisting of R16/P2, was applied to the input of the programmable reference TL431 (Q2) which was used as a high gain comparator. When the output voltage increases above the 5 V value, the TL431 turns on and forward biases the LED of the optocoupler which, in turn, forces more current into the node built around R2/R5/R7. This current develops a feedback voltage across R5 reflected back to the MC44602P2 by resistor R7. The regulation loop is now closed and the SMPS driver will take the necessary action to set the output voltage at the right value. The same mechanism applies, in the opposite direction, when the 5 V output voltage decreases below the value adjusted by potentiometer P2.

In addition to the galvanic isolation, the critical points with the optocoupler are:

Optical to current transfer ratio absolute value
Transfer ratio linearity

The M0C8101 has been specifically designed to cope with the converter applications, providing the designer with a low gm dispersion and excellent linearity as shown by the electrical specifications of this device.

Voltage regulation can be accomplished by sensing the Vaux value with the R20/P1/R21 network as depicted in the schematic diagram. In order to provide more flexibility in the implementation and analysis of the power supply, the regulation mode is selected by jumper S1 or S2:

S1 : Internal regulation (V_{aux})
S2 : External regulation (Optocoupler)

Input Rectifiers and Filtering

Selecting the input line rectifiers is straight forward and needs no particular discussion. Four MR506 rectifiers capable of sustaining the maximum line voltage and inrush current at start up were used.

Since the minimum V_{CE} voltage under the worst case conditions is 262 V (V_{line} minimum and full load), the input filter capacitor was computed by assuming a ripple voltage equal to 12% of the rectified line voltage. Under these conditions, the capacitor was derived from equation [30]:

$$C = \frac{P_{out}}{2\partial(Fl)(\Delta E_j)} \quad [30]$$

with: C = input capacitor in Farad
Fl = line frequency in Hz
∂ = global efficiency in %
ΔE_j = energy supplied by the capacitor
The ΔE_j is given by equation [31]:

$$\Delta E_j = (0.5C)(V_{CE(high)}^2) - (0.5C)(V_{CE(low)}^2) \quad [31]$$

$V_{CE(high)}$: peak rectified line value
$V_{CE(low)}$: minimum rectified line voltage at the end of one line cycle

then:

$$C = \frac{300}{(080)(50)(291^2 - 260^2)} = 439\ \mu F$$

Two 220 µF/385 V capacitors in parallel were used (C15 and C16).

A standard L/C filter (a π configuration) was mounted in series with the line wires to minimize the RFI noise generated by the power supply on the line wiring. This filter also damps the voltage spikes that may exist on the main line.

PERFORMANCE ANALYSIS

Voltage Regulation

The voltage regulation measurements were performed with the opto coupler connected to the 5 V output. The results are summarized in Tables 3A, 3B, and 3C. It must be pointed out that the 100 V output had no post regulation and no particular effort was made to improve the cross regulation.

Table 3.A. V_{out} Regulation as a Function of the 5 V Load (V_{line} = 220 V)

I_{out} @ +5 V	5 V Output	100 V Output
2 A	5.31 V	60 V
5 A	5.28 V	78 V
10 A	5.27 V	88 V
20 A	5.25 V	91 V
30 A	5.20 V	94 V

Table 3.B. 100 V Output Voltage Regulation as a Function of Load (V_{line} = 220 V)

I_{out} @ +100 V	+100 V Output
0.5 A	94 V
0.8 A	94 V
1.0 A	94 V
2.0 A	91 V

Table 3.C. Output Voltage Regulation versus Line Voltage (Load = 250 W)

V_{line}	5 V Output	100 V Output
185 V	5.22 V	94 V
220 V	5.20 V	94 V
265 V	5.21 V	94 V

The load and line regulations were excellent for the 5 V output, however the cross regulation of the 100 V output could be improved by a redesign of the output transformer and the associated output filters network.

Foldback

The MC44602P2 is designed to provide a power foldback when the load exceeds the maximum limit specified by the designer. The slope of that characteristic is a function of the current flowing out of pin 3 as defined by the data sheet. Figure 10 shows the current foldback characteristic of the 300 W converter.

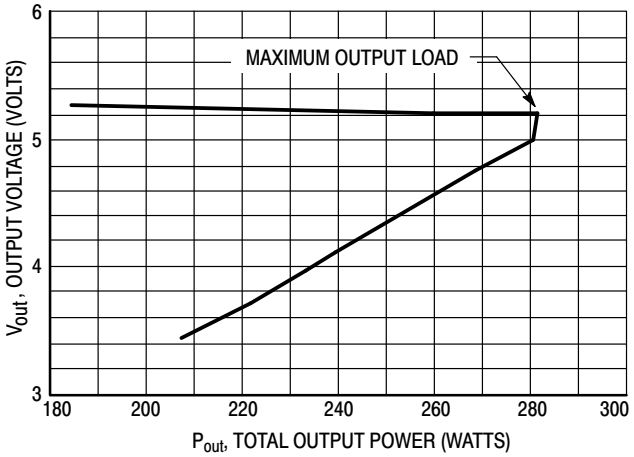


Figure 10. Foldback Characteristic of the 300−W, 100−kHz Converter

Short Circuit Protection

By sensing the voltage across the auxiliary winding, the driver provides short circuit detection, yielding full protection of the output switch. Moreover, the MC44602P2 takes care of the magnetizing of the output transformer prior to re−starting the converter. This ensures the power switch will not exceed its FBSOA at turn on. Since the converter operates in the Forward mode, the auxiliary winding is out−of−phase with the output voltages; and the short circuit protection mechanism, as defined by the driver's data sheet, cannot be used. Therefore, the current limit feature was used to turn off the converter in case a short circuit occurs across one of the outputs. Since it was not possible to take advantage of the built−in short−circuit protection, the transistor must be sized to sustain the large FBSOA required during this overload.

Bipolar/MOSFET Comparison

For comparison purpose, the same circuit has been operated with the MJW18010 bipolar transistor and the MTW7N80E MOSFET (7 A/800 V). The global efficiencies were measured under several load conditions for a constant line voltage. The results are given in Table 4. Since there was no power factor correction built into the power supply, the power factor was 0.62 under the full load.

Table 4.Global Efficiency at V_{line} = 220 V

Total Load	MJW18010	MTW7N80E
50 W	86.2%	78.1%
90 W	84.7%	83.3%
135 W	86.4%	76.74%
185 W	85.8%	80.3%
250 W	84.5%	82.5%
300 W	83.7%	83.7%

After four hours of continuous operation, the temperature of the power components (both active and passive) were measured and are shown in Table 5.

Table 5.Power Elements Steady State Temperature (250 W load, @ T_{amb} = 22°C)

MJW18010	74.7°C*	100 V Output Filter Core	45.4°C
MBR28045 V	62.3°C**	15 V Post Regulator	50.3°C***
MUR480E Clamp D	50.2°C*	Output Transformer Core	62.5°C
5 V Output Filter Core	45.2°C*		

Notes: *Heatsink is 9°C/W
**Heatsink is 0.6°C/W
***Heatsink is 18°C/W

These results demonstrate that no thermal run away will occur, even if the ambient temperature rises up to 50°C.

With a nominal efficiency of 84.5%, the losses represent 44 W dissipated in the circuit (under a 240 W load, the input power was 284 W). Most of these losses can be computed and predetermined (particularly the ones in the semiconductors); however, the non-negligible part can only be estimated, therefore, it is more difficult to improve.

As a reference for a global efficiency improvement, Table 6 shows the losses, as computed, for the most critical parts in the power supply.

Table 6.Sources of the Losses in the Power Supply (Bipolar driven)

MJW18010	on time	2.00 W
	turn off:	3.30 W
Base Network		3.50 W
MBR28045V		16.50 W
MURH840		3.20 W
MC44602P2		0.35 W
Snubber Network		9.32 W
Total:		41.17 W

The remaining 3 W are dissipated in the ferrites, windings, filter capacitors and the line network. These losses may be minimized, but the cost of such improvement may be too expensive for a 1% efficiency improvement.

Measurements and Oscillograms

The MJW18010 exhibits an extremely fast turn-off time as shown in Figures 11 and 13. With a collector current fall time of 60 ns, this bipolar transistor was comparable to the MOSFET which has its switching speed shown in Figure 12.

The Baker clamp, in conjunction with the planar transistors, yields a storage time as low as 0.5 microsecond under the worst case condition, which made possible efficient operation of the power supply over large load variations.

In the dynamic $V_{CE(sat)}$ waveform depicted by the oscillograms, note the curves include the forward drop V_f of the diode used to sense this voltage (see the test circuit and waveform shown in Figure 14).

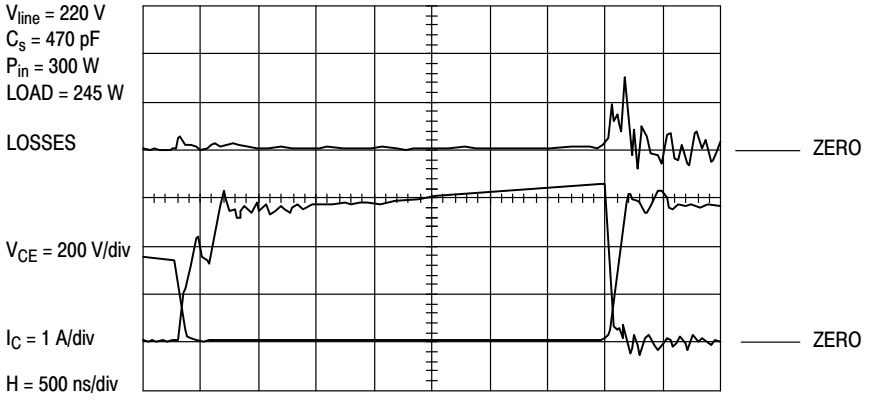


Figure 11. Losses in the Bipolar Transistor

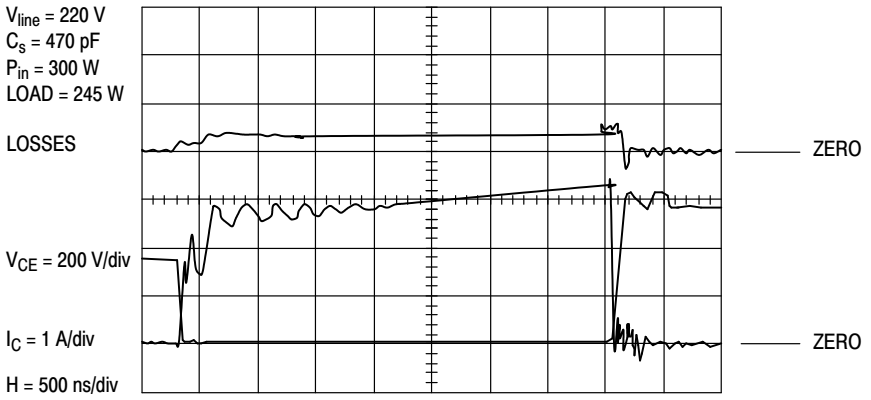


Figure 12. Losses in the Power MOSFET

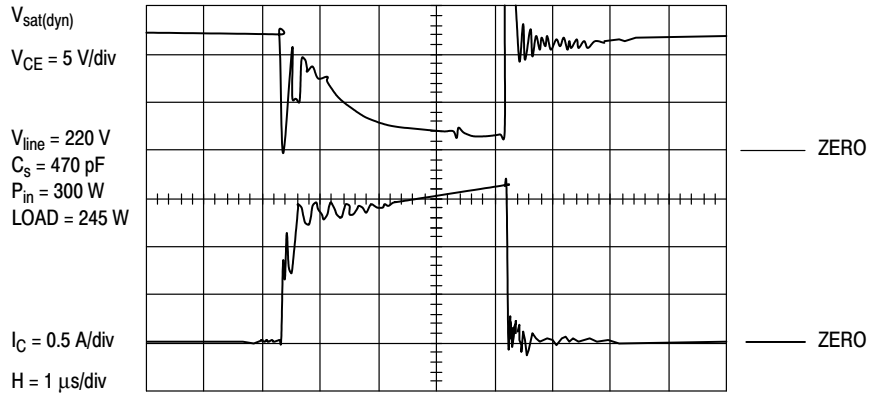
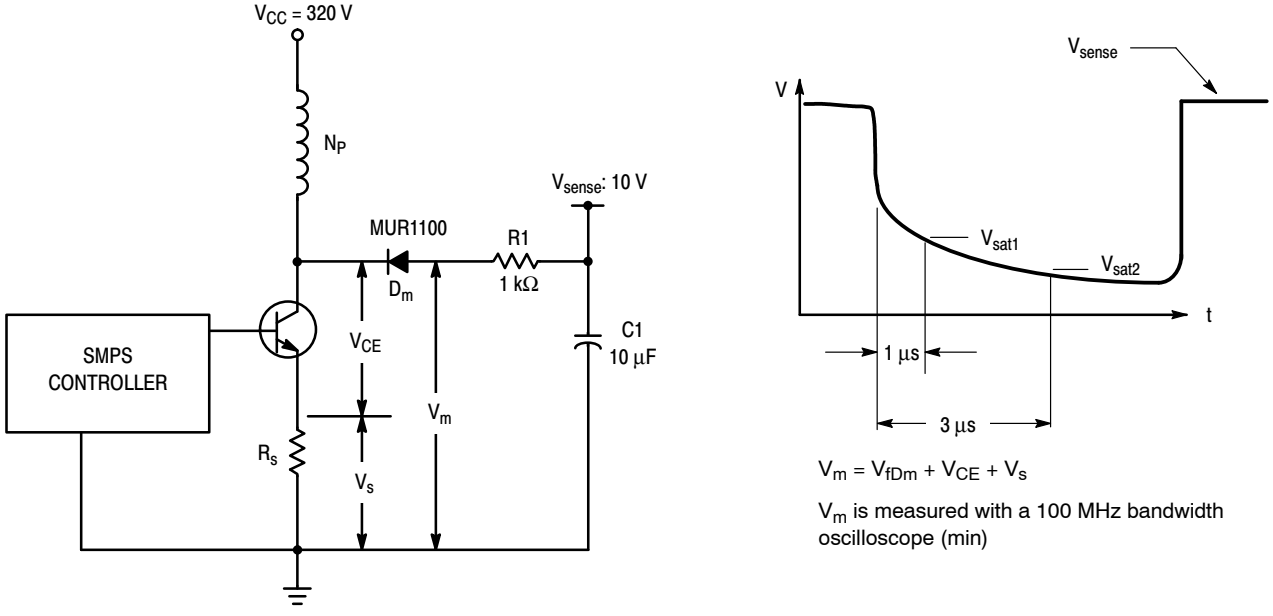


Figure 13. Dynamic $V_{CE(sat)}$ of the Bipolar Transistor



$V_m = V_{fDm} + V_{CE} + V_s$

V_m is measured with a 100 MHz bandwidth oscilloscope (min)

Figure 14. Dynamic On-voltage Test Circuit

The equivalent MOSFET is the MTW7N80E with a BV_{DSS} of 800 V, is energy rated and has a drain current rating of 7 A. The typical $R_{DS(on)}$ is 0.85 Ω @ T_J = 25°C at I_D = 3.5 A). The MOSFET die is 82% larger than the MJW18010, more expensive than the bipolar device, and did not provide the designer any significant advantages. Even the dynamic performance of the two products were similar.

From a total power loss point of view, the high on-voltage of the MOSFET defeated the benefit of its fast current fall time. The case temperature, measured under the same conditions as defined for the bipolar transistor, was 103.4°C after four hours of continuous operation. Such a high temperature is undesirable in most applications because the designer must use expensive solutions, such as a larger heatsinks or forced air cooling, to keep the operating temperature at a safe level for long term reliability.

Most of the losses of the MOSFET were generated in the on-state by $R_{DS(on)}$. The switching loss of the MOSFET was about one third of the MJW18010. A typical $R_{DS(on)}$ of 1.80 Ω at T_J = 100°C yields on-losses calculated as follows:

$$P_{on} = R_{DS(on)} I_D^2 DC_{max} \quad [32]$$
$$P_{on} = (1.80)(3^2)(0.50) = 8.10 \text{ W}$$

The gate drive needed much less energy than the base-to-emitter network of the bipolar device and at an operating frequency of 100 kHz, can be neglected as shown below:

$$P_{drive} = 0.5 C_{iss} V_{gs}^2 F \quad [33]$$
$$P_{drive} = (0.5)(2900 \times 10^{-12})(12^2)(10^5) = 208 \text{ mW}$$

With a drain current fall time of 20 ns, the turn-off losses were equal to 1.20 W, yielding a total of 9.50 W dissipated by the MOSFET. This is nearly 50% above that generated by the bipolar transistor and confirms why a higher ΔT_J occurs with the MOSFET. The primary advantage of the MOSFET was the ease of drive with no need of an external circuit to control the operating point for load variations.

CONCLUSIONS

A switching power supply was designed utilizing the new high voltage planar transistors and demonstrated they are a good alternative in a 300 W forward converter. Bipolar transistor solutions should not be overlooked in SMPS using the forward converter topology and if within the power range of the circuit described in this Application Note.

Yielding an efficiency greater than 84 percent and voltage regulation better than 1%, the power supply utilizing the bipolar transistors met the original target specifications.

MOSFETs are a good alternative, but high voltage devices result in high conduction losses. They are more expensive when compared to equivalent bipolar transistors because more silicon is required to achieve equivalent performance. In this case, the bipolar solution was a better choice.

The use of modern rectifiers, like the MEGAHERTZ™ Series and Schottky rectifiers in conjunction with the new MJW18010 bipolar planar transistors, enables the design of cost effective, efficient, high current, high frequency converters.

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PUBLICATION ORDERING INFORMATION

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